Design of a silicon on insulator pixel detector using a charge sluice

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Abstract

Silicon on insulator (SOI) technology allows for the production of pixel detectors that have greater efficiency and resolution at lower costs. We have modeled an SOI detector pixel which uses the concept of a charge sluice, in which we attempt to transfer charge from one p-doped well to another, in order to reduce the parasitic capacitance while at the same time maintaining a uniform field within the device. After varying multiple parameters related to both the physical structure and voltages at the various electrodes, we have been unable to get this design to work, since the deposited charge tended to spread itself out to equalize the potentials in both wells.

I. Introduction

Silicon on insulator (SOI) technology allows for the creation of improved pixel detectors for use in future experiments. This technology enables the pixel detectors to have radiation hardness, to be more compact, to be more cheaply manufactured, to have greater detection efficiency, and to work over a greater range of temperatures.[1, 2, 4, 5] SOI refers to the placement of electronic systems almost directly on top of a silicon substrate, with only a layer of insulator in between (see Figure 1), as opposed to the typical construction where the two components are joined by a solder blob. A high-energy particle will ionize atoms in the substrate, and the electrons will flow to a positive electrode at the bottom of the substrate, while the holes left behind will go toward a detector at the top of the substrate, with appropriate readout electronics built on top of the insulating layer. In order for this to successfully work, a number of p-doped wells are placed near the surface of the substrate, which serve to attract the holes.[2, 6] Complicating things is the fact that the electronics on top of the insulator can have an influence on the substrate, leading to the creation of holes unrelated to the detection of a particle. In order to prevent this, it has become common to insulate the surface electronics by means of nested wells. In particular, an n-doped well (n-well) is placed directly beneath the electronics, with this well surrounded by a p-doped well (p-well). The potential barrier between the two regions serves to insulate the electronics from the rest of the substrate.[2, 6]

Another problem with these detectors is the well size. It is desirable to have the field in the substrate uniform, so that holes created by the passage of a particle will be pulled directly up with minimal lateral motion. To accomplish this, it is necessary that the p-well connected to the readout electrode be large. At the same time, we want a small capacitance from this p-well, which would require us to make the well small.[2] To resolve these issues, Deptuch et al.[3] have proposed

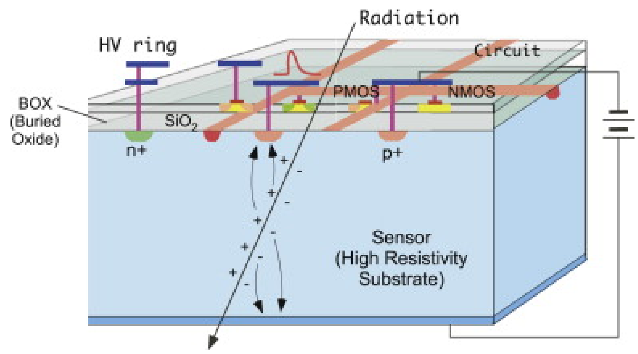

FIG. 1. Basic structure of an SOI pixel detector. The buried oxide layer on top serves as an insulating layer. Source: Arai et al.[1]

the creation of a charge sluice. This design, shown in Figure 2 calls for the creation of two well structures. One would consist of a large buried p-well surrounding an n-well. This would insulate the substrate from the electronics in the manner described above. It would also serve to collect holes from the ionization caused by the particle we wish to detect. The other well structure would be a buried n-well surrounding a small surface p-well, to which the detector electrode would be attached. This n-well would prevent charge from accumulating on the surface p-well except by a p-doped channel between this surface p-well and the buried p-well. An electrode placed above this channel would allow us to lower its potential, permitting charge to flow between the two wells, or raise it, blocking this flow. In this manner, we could allow charge to accumulate on the buried p-well and periodically send this charge over to the surface p-well by means of the charge sluice. This procedure would enable us to have our charge collected on the large p-well, with its uniform electric field, but detected at the small p-well, with its low capacitance.

In order to determine how well this idea would work, we modeled the structure in ATHENA and then ran simulations using ATLAS, two electronics programs produced by SILVACO. ATHENA allows one to create a model of an electronic component using methods similar to those used in the device's actual construction.[7] ATLAS simulates the behavior of an electronic device by determining the fields inside the device and using these to model how charges move.[8] In order to interpret the data, we used Tonyplot, a SILVACO program which plots the outputs of ATHENA and ATLAS.[9]

II. Methods

We built a model of the pixel detector in ATHENA and simulated it using the ATLAS software. For ease of learning and convergence, we used the two dimensional versions. To make the structures, we created a lightly n-doped silicon substrate. We then added a layer of silicon dioxide on top to help insulate the substrate and surface electronics from one another. To dope certain regions of the silicon as wells, we covered all of the substrate with a photoresist mask, except the areas which we wanted doped. We then implanted our dopant at a certain energy to get it to reach the desired depth. We removed the photoresist and repeated. We finally added in electrodes by etching out parts of the silicon dioxide and filling the space with aluminum.

We used ATLAS for our simulation. Since we wanted our detector to be able to detect ionization in the substrate due to the passage of energetic particles, we used the single event upset model in ATLAS, which creates a number of electron-hole pairs in a given region according to user

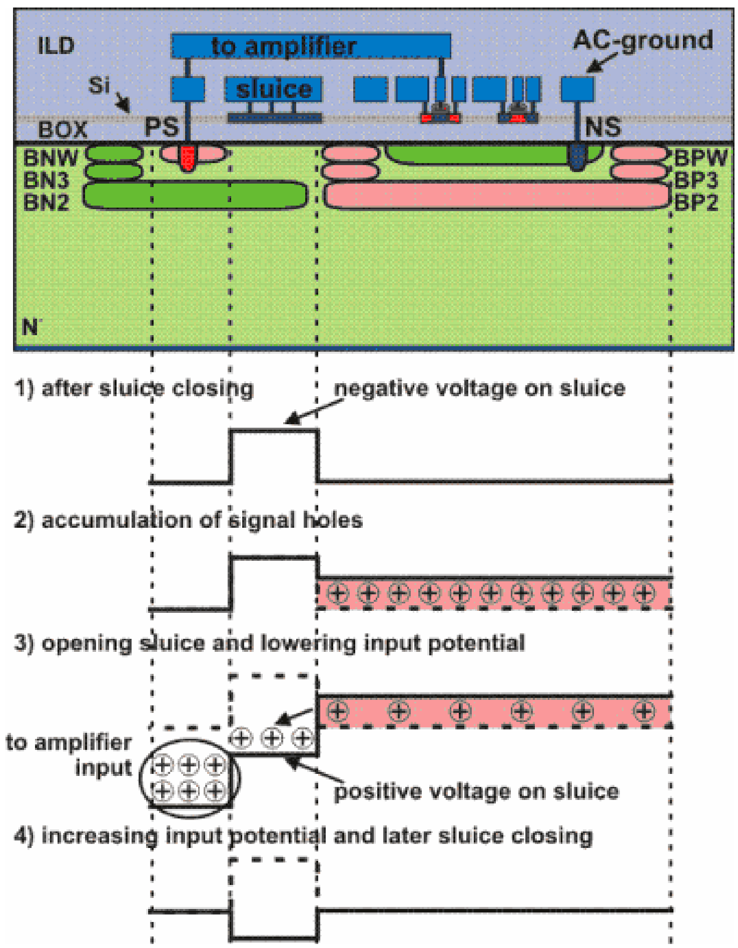

FIG. 2. Design for a charge sluice. Source: Deptuch et al.[3]

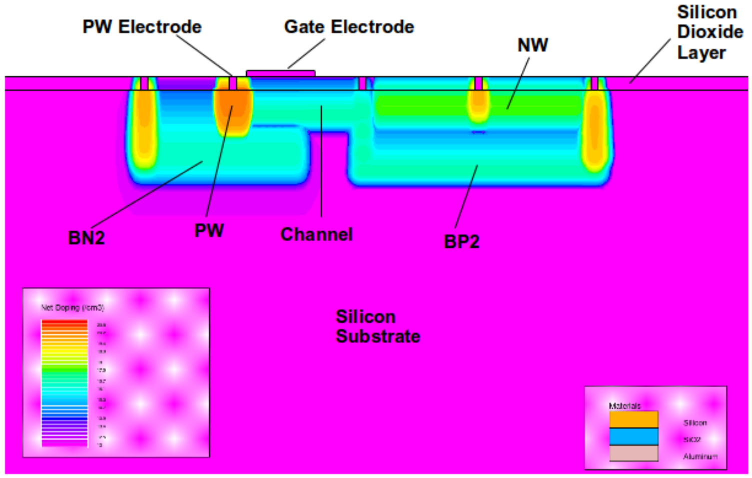

FIG. 3. Basic design of our pixel detector. Wells labeled with "N" are n-doped, while those labeled with "P" are p-doped. The width of the device is 55 microns and the height is 6 microns for the silicon substrate, with an extra 200 nm for the oxide layer on top.

specifications. We initially used depositions of 4300 and 870 electron-hole pairs to test our design, since we wanted our detector to be able to operate with ionizations involving 1000 to 4000 electrons. However, as our work progressed, we became more interested in small-signal analysis, causing us to lower the ionization to 87 or 870 electrons. In order to determine our backgrounds so that they could be subtracted out, we also ran simulations in which no ionization occurred.

Our first concern was to get the charge sluice to effectively transmit charge from the collection well (bp2) to the output well (pw). (See Figure 3.) We therefore ran a series of simulations in which we started off with the gate electrode at a high potential, so that the channel would be impassable. In this mode, all the deposited charge would flow to and collect in bp2. We then lowered the potential on the gate electrode to make the channel passable and permit the electrons to flow from bp2 to pw and into the pw electrode. In order to determine the charge seen by pw, we integrated the current seen by the pw electrode for simulations in which charge was deposited and subtracted the integrated current obtained in the simulations in which no charge was deposited. In order to prevent charge from being collected by the bp2 electrodes, we set the resistance associated with them to be large, essentially disconnecting them. In order to determine the total charge deposited, we examined the SEU Track Cumulative Charge in Tonyplot.

Our other initial concern was how well the gate was able to separate the two wells. We therefore wanted as little charge as possible to flow into pw before the gate potential was lowered. In order to measure this, we integrated the current into the pw electrode only during the time when the gate was at its high voltage (5 V) and compared the values obtained when charge was deposited to those when it was not.

We were also interested in the capacitances of the detector. In our initial attempt to determine this, we tried to run ATLAS in AC mode, in which an AC signal would be generated at one electrode and the capacitance between that electrode and any other, along with other variables, could be measured. This required the specification of a frequency at which to conduct this analysis. Since we were turning the gate electrode on and off with a frequency of 25 MHz, we chose to use that value for our capacitance analyses. However, we realized that this did not give us the capacitance which we were looking for, since we wanted to see the voltage generated by some charge traveling through the structure, while this method told us the capacitance that would be seen by some non-existent AC signal. We therefore calculated capacitance directly by running the simulation and seeing what the increase in potential was at the pw electrode. Unlike the simulations run to ensure that the gate was working, we set the resistance on the pw electrode to be very large, essentially making it a floating electrode, since it was necessary to let the charge build up in pw so that we could see a voltage, rather than collecting it as soon as it came in. Our simulation then had the following stages: deposit the charge and run for 20 ns with bp2 and pw disconnected so the charge can collect in bp2. Then, connect the two wells for 20 ns, so charge could flow into pw, then disconnect them again so that pw would be one small isolated well for low capacitance. At this point, we read out the voltage in pw. Finally, we lowered the resistance at the pw electrode so that we could measure the current through it and thereby verify how much charge we had actually collected. As before, we ran each simulation with 870, 4300, and 0 electron-hole pairs deposited so we could monitor the detector's behavior at both extremes of signal and so that we could subtract off the dark-current.

As we progressed, we ran into a number of problems with this approach. Following this approach, we were able to obtain very low capacitances. However, we eventually realized that the charge we had been seeing was not actually the deposited charge; we had set up a voltage difference between bp2 and pw, resulting in a current between them. The deposited charge was modifying the behavior of this current, resulting in the appearance that our deposited charge was flowing into pw. While in theory it might be possible to use this phenomenon as a proxy for charge detection, in practice, it would introduce large errors into our readings on account of the natural variability of the current. In addition, there would be trouble oscillating the voltage at the gate electrode quickly enough to take advantage of the differences in the behavior of this current. At this point, we also set the electrode at the bn2 electrode to be at a high resistance to simulate how this device would work in practice.

In order to avoid this current, we made sure that pw and bp2 were starting at the same potential. To do this, before any charge was deposited, we lowered the voltage on the gate electrode to make the channel passable and allow the voltages between the two wells to become equal. We then made the channel impassable again and deposited our charge. Since there was no longer any voltage difference between the two wells, transferring our charge became an issue. We reevaluated the channel doping, and found a level where we could make the channel passable or impassable even with no voltage difference between the wells.

Since this approach did not yield any improvements over the capacitance obtained without a charge sluice, we tried a new method. We set pw to a lower potential than bp2, but only lowered the potential on the sluice partway. Our hope was that the voltages in the two wells would try to equalize, but they would not be able to due to the fact that, when the potential in bp2 had become lower than that of the channel, no more charge would flow between the two, even if their potentials were still not equal. By choosing to lower the channel to the right potential, we could make it so that the only charge that would be able to flow over would be the charge from the ionization, and, since it would want to try to equalize the potentials in the two wells, but there would not be enough mobile charge to do so, all the ionized charge would go into pw.

While taking all these measurements, we varied all sorts of parameters related to both the physical structure of the pixel detector as well as the voltages on the various electrodes and the times when they were changed. In order to efficiently run these simulations, we wrote our code so that variables could be easily changed.* By replacing the desired value with some variable, we were able to cycle through a number of values without human intervention, allowing overnight

*We were more careful with this parameterization in ATHENA than in ATLAS, since the code in the latter was shorter and more regular, so that it was not hard to just scroll through it and change the appropriate values.

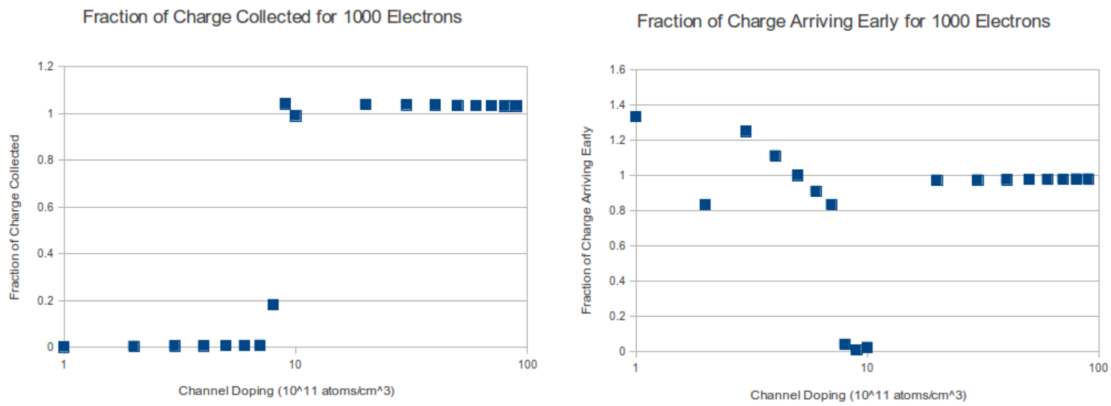

FIG. 4. Fraction of deposited charge detected and fraction of detected charge arriving early (while wells are supposed to be disconnected) with 870 electron-hole pairs deposited.

experiments. In order to work even more efficiently, we wrote a shell script to run a series of different experiments overnight or through weekends.

III. Results

To get the gate to work properly, so that nearly all the charge would flow in when we lowered the voltage on the gate electrode, but so that no charge would flow before then, we tried varying a host of parameters in the design. In the end, the most effective was the doping in the channel. If we had too little doping, charge would never flow between the two wells, but, if it was doped too much, the gate electrode would be unable to make a significant barrier between the wells without using an absurdly high voltage. We therefore ran an experiment to determine the proper value and recorded what fraction of the deposited charge was ultimately detected and what fraction of the detected charge was detected early, while the channel was still supposed to be blocked. The results are shown in Figure 4 and Figure 5. The reason that some of the values are over 1 is probably account of numerical errors, or perhaps there are small effects which we do not fully understand. The increase in the fraction of charges arriving early at low doping is on account of the channel being blocked to all charges, so the small number that are detected did not take the channel, and therefore did not care that it was blocked. Based on these data, we decided to dope the channel at $9 * 10^{11}$ atoms/cm^3.

At this point, as described previously, we realized that, in order to accommodate studies of capacitance, it was necessary to keep the electrode at pw at high resistance. However, by setting it initially to a lower voltage than those at bp2, we were able to induce a current between the two wells, the behavior of which was modified by the deposition of charge, as seen in Figure 6, Figure 7, and Figure 8. Specifically, in the end, this background current always served to equalize the voltages in pw and bp2. However, the deposition of charge increased the current, so that this equalization occurred more quickly than in cases without charge deposition.

Due to the variability of this current in a real device, this method would introduce considerable errors into our measurements. In addition, a reference to Figure 6 and Figure 8 shows that, if we want to take advantage of this difference in the behavior of the current, we need to keep the gate at low voltage for a very short time (~20 ns), which would be difficult for the electronics to accomplish.

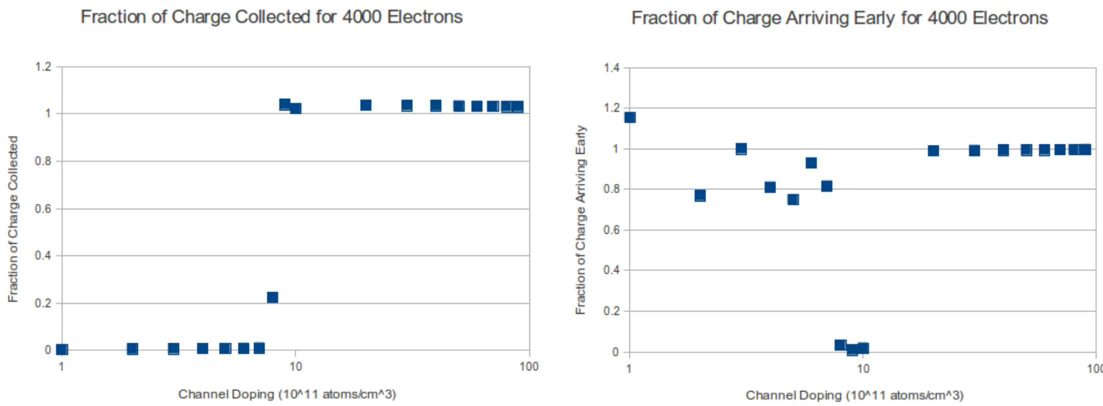

FIG. 5. Fraction of deposited charge detected and fraction of detected charge arriving early (while wells are supposed to be disconnected) with 4300 electron-hole pairs deposited.

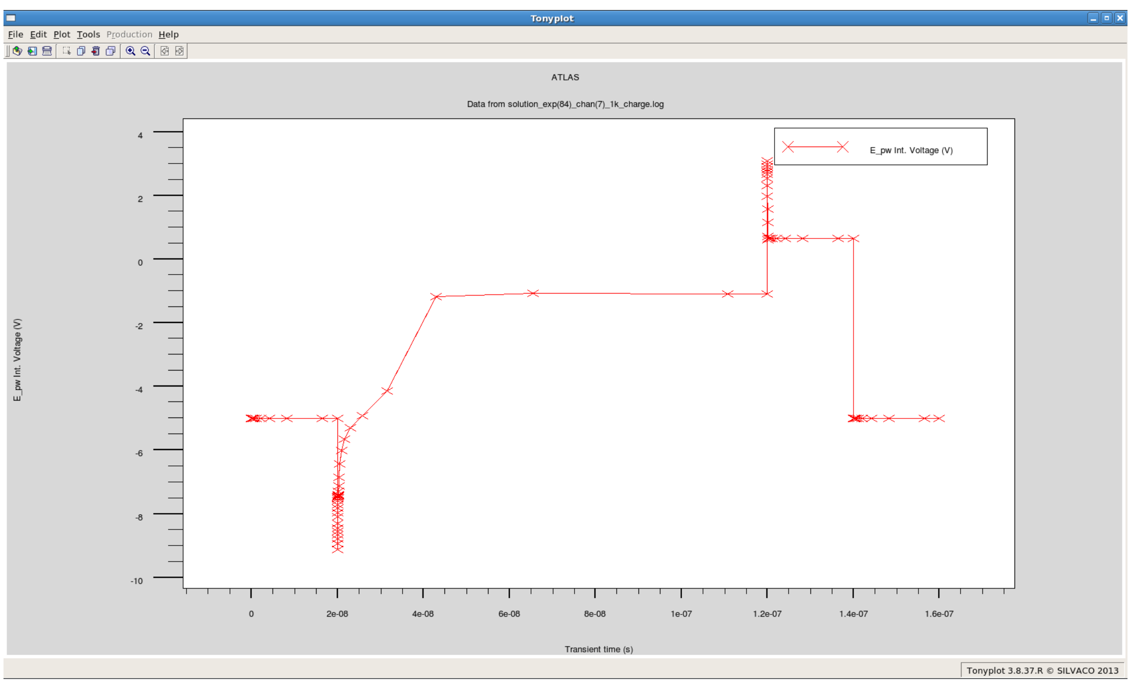

FIG. 6. Voltage in pw as a function of time for 870 electron-hole pairs deposited. Compare with Figure 8. Note how it ends at roughly the same voltage, but the current is greater at the beginning, then levels off.

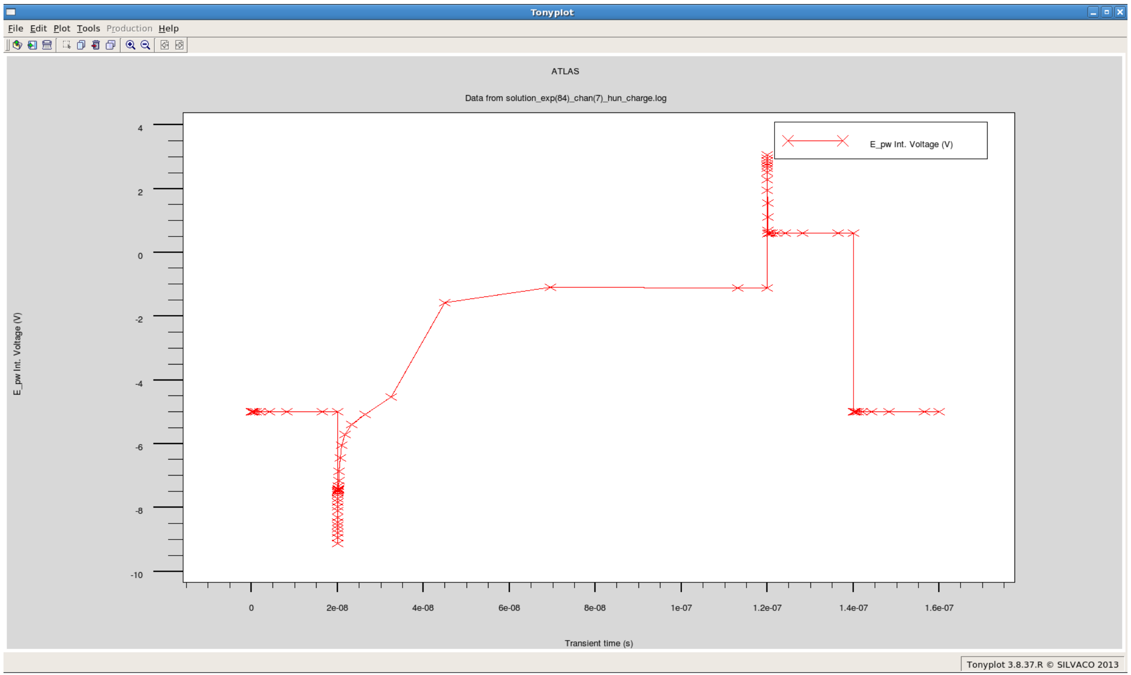

FIG. 7. Voltage in pw as a function of time for 87 electron-hole pairs deposited. Compare with Figure 8. Note how it ends at roughly the same voltage, but the current is greater at the beginning, then levels off, similar to the case of 870 electrons, but to a lesser degree.

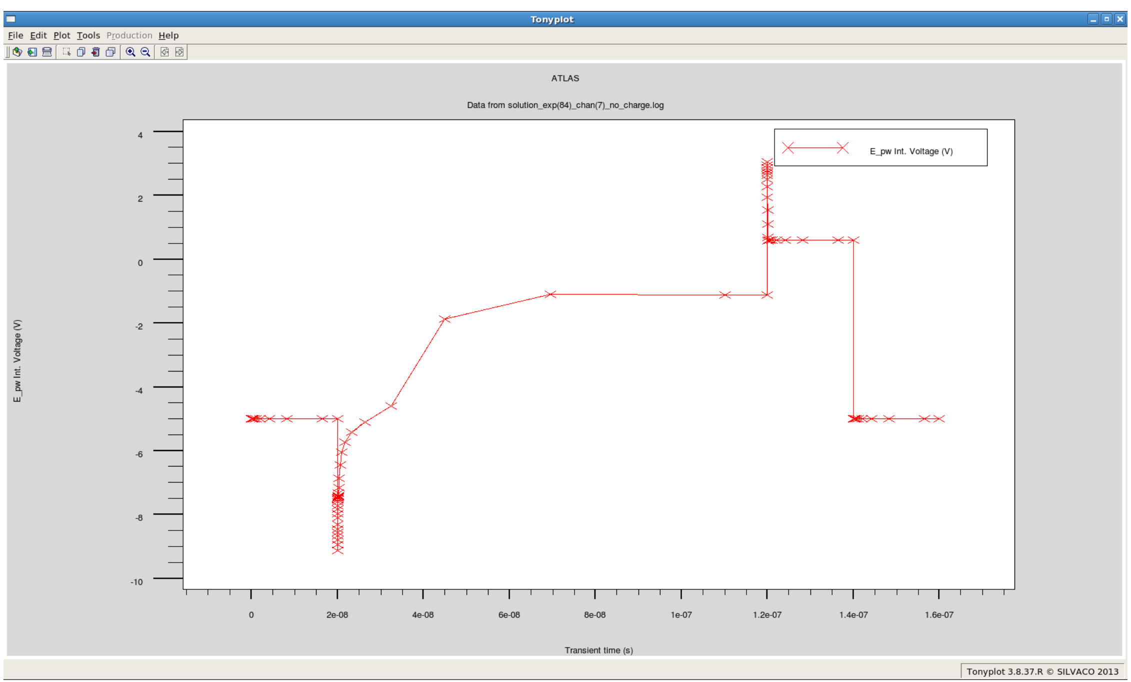

FIG.. 8. Voltage in pw as a function of time with no charge deposition. Compare with Figure 6 and Figure 7. Although the same final voltage is reached, the current causing this change is lower and longer-running than in the other two cases.

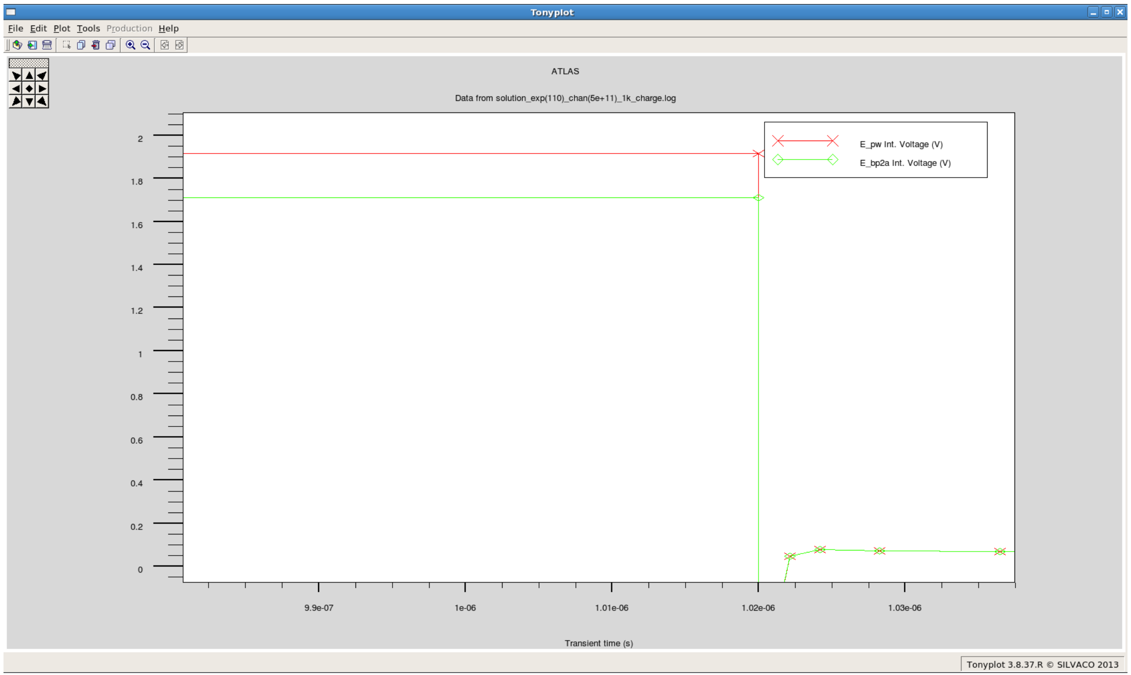

FIG. 9. Channel is made passable at 1.02 μs. Note how both pw and bp2 go to the same potential.

In order to avoid such problems associated with these background currents, we eliminated any voltage difference between the two wells. However, with no voltage difference, charge spread through the available area to cause an equal increase in voltage in both wells. This may be seen in Figure 9. If this was indeed the situation, and not just a numerical coincidence, we would expect that, as we increased the size of pw, more charge would flow into it in proportion with the ratio of its size to that of pw plus bp2 $\left(Q_{pw} \propto \dfrac{width_{pw}}{width_{pw} + width_{bp2}}\right)$. We performed this experiment, and found that as the size of pw is increased, the charge collected increases in proportion with the ratio of the size of pw to the size of both wells combined. This may be seen in Figure 10.

To try to prevent this equalization of voltage between the two wells, we reintroduced a potential difference between the two wells, but only lowered the channel potential partway, as described previously. Varying the low voltage on the gate electrode gave us the data shown in Figure 11. It is easy to see that there is no point where we get our drastic lowering of the capacitance, but rather, just an asymptotic falloff to the voltage of bp2 without a charge sluice.

IV. Conclusion

During the course of our project, we were unable to use a charge-sluice to reduce the capacitance of our pixel detector. The reason appears to be that, whenever we permitted the flow of charge between the two p-doped wells, the voltages in them would equalize, preventing us from collecting the majority of the deposited charge in the small surface p-well, as we would have liked. Perhaps a creative solution in the future will be able to overcome this barrier.

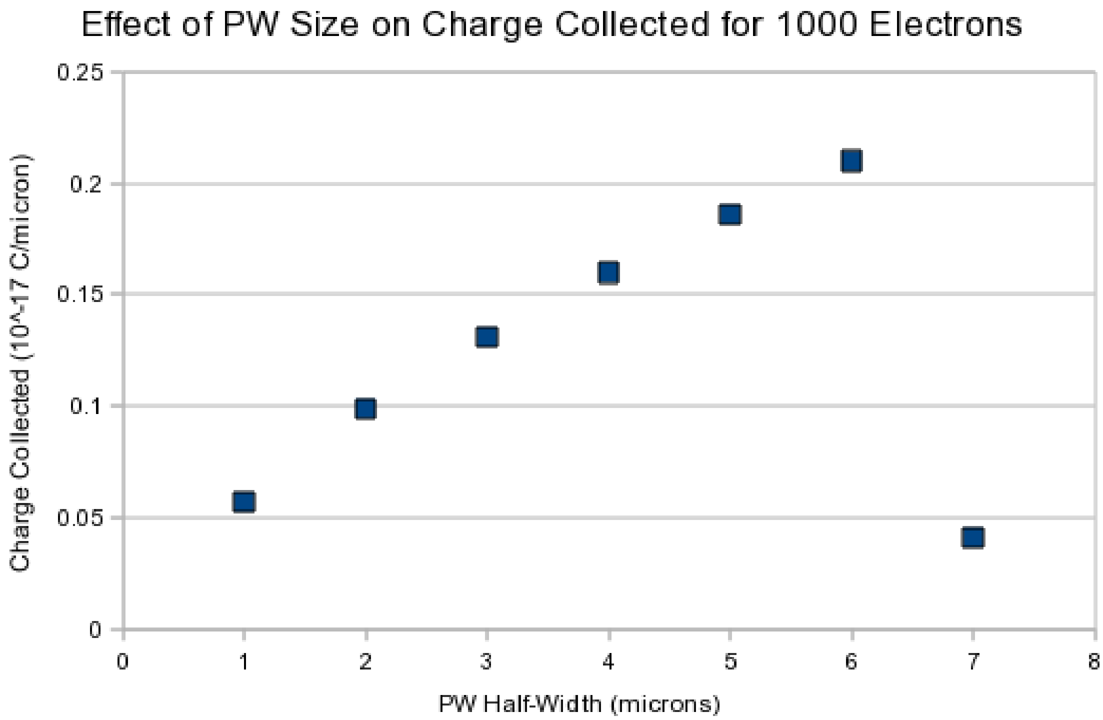

FIG. 10. Charge collected increases in proportion to ratio of the size of pw to the size of pw plus the size of bp2, as we would expect if charge is spread through both wells to equalize the voltage.

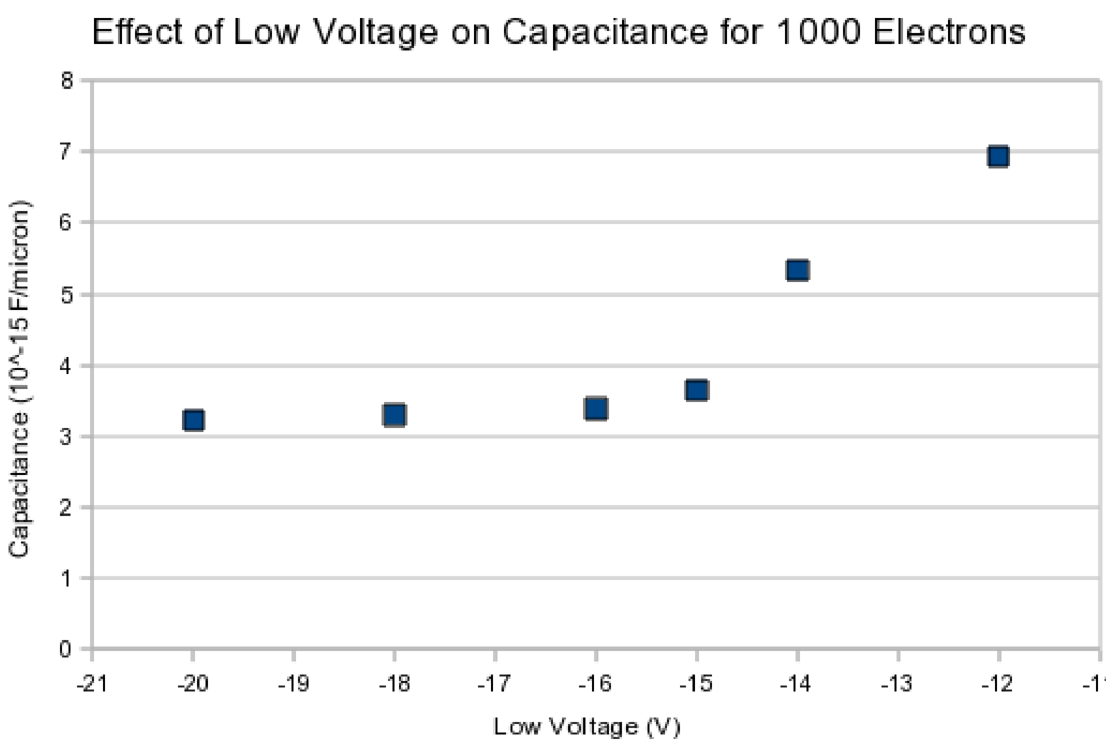

FIG. 11. As we lower the potential in the channel, we are able to get more charge to flow through until we reach the voltage of bp2 without the charge sluice.

V. Acknowledgements

I would like to thank Grzegorz Deptuch and Farah Fahim for teaching me the necessary skills to complete this project and providing invaluable guidance along the way. This work was supported in part by the U.S. Department of Energy, Office of Science, Office of Workforce Development for Teachers and Scientists (WDTS) under the Science Undergraduate Laboratory Internship (SULI) program.

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